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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/191,629	11/13/1998	THANH T. TRAN	A98289US	8851

7590 02/25/2005

IP Adminstration, Hewlett-Packard Company
Legal Department MS 35
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EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/191,629	TRAN ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,8-18,20-24,34-38 and 40-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *52 and 84* is/are allowed.

6)☒ Claim(s) *1-4,6,8-18,20-38,40-43 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Upon further reconsideration and careful review, the previously indicated allowability of claim 44 has been withdrawn. Examiner regrets the inconvenience this may cause the applicant.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-4,6, 8-18, 20-24, 34-38, 40-46** are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye, U.S. Patent No. **6,067,098**.

Considering claim **1**, Dye discloses the following claimed subject matter, note;
c) the claimed method of monitoring a feedback signal provided by a graphics controller coupled to the system, the monitoring by the interface logic and the feedback signal indicates whether a programmed position of a display device has been refreshed, is met by the CPU 102, and the Integrated Memory Controller 140, fig.3, which together control how the data is displayed on the screen, since without the programmed position being monitored by a *feedback or sync signal* of the controller (which in turn is under the control of the CPU), *the position of the contents of the display screen or window (the DTV data) may not be controlled on the screen.*

d) transmitting the outgoing frames of digital television data in the second frame buffer to the graphics controller to be displayed on the display device when the programmed position of the display device is refreshed, is implied because the controller 140 reads/writes from the system memory (i.e., the virtual frame buffer). (col. 21, lines 22-25).

Except for;

a) the claimed method of storing incoming frames of digital television data in a first frame buffer of an interface logic;

b) the claimed method of reading outgoing digital television data from a second frame buffer, of an interface logic;

Regarding (a) and (b), Dye discloses that "The IMC 140 uses techniques to improve overall system performance and user response time by use of the main system memory as a virtual graphical frame buffer and program/data storage. The IMC 140 provides a unique system level architecture that reduces data bandwidth requirements for general media input/output functions. Because the host CPU 102 is not required to move data between main memory and the graphics and audio and telephony subsystems as in conventional computers, data can reside virtually in the same subsystem as the main memory. Therefore, for media output data (audio, video, telephony) the host CPU or DMA master is not limited by external available proprietary bus bandwidth, thus improving overall system throughput." (Col. 11, lines 52-65)

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to implement the system of Dye by utilizing the system memory for both incoming and outgoing frames of television signals instead of using separate frame

buffers for storing incoming data and for storing outgoing data, so that the system as whole is made more compact and less costly.

Considering claim **2,** Dye discloses the following claimed subject matter, note; storing the incoming frames of digital television data in the second frame buffer; reading the outgoing frames of digital television data from the first frame buffer; transmitting the outgoing frames of digital television data in the first frame buffer to the display device when the programmed position of the display device is refreshed.

Regarding claim 2, see rejection of claim 1(a),(b) and (d), respectively.

Considering claim **3,** the claimed method of detecting whether the outgoing frames of digital television data is stored in the first frame buffer or the second frame buffer, is met by the CPU 102, fig.3.

Considering claim **4**, the claimed method of monitoring step comprising the step of monitoring a horizontal sync and a vertical sync of the display device, is met by the disclosure "The IMC 140 couples to a display device 142, such as a computer video monitor or television screen, among others. The IMC 140 generates appropriate video signals for driving display device 142. The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142. The IMC 140 also generates NTSC video signals, PAL video signals, or video signals for other analog or digital television/video formats. The IMC 140 may generate any of various types of signals for controlling a display device or video monitor. As shown, the IMC 140 preferably uses a serial control

bus, such as the I2C serial bus, for control of the display device 142." (col. 10, lines 46-58)

Considering claim **6**, Dye discloses all claimed subject matter, except for;
The claimed method of transmitting the outgoing frames of digital television data over a peripheral component interconnect (PCI) bus, is met by PCI/USB busses, Fig.2A and 2B.

Considering claim **8**, Dye discloses the following claimed subject matter, note;
a) a central processing unit (CPU), is met by CPU 102 (fig.2A).
b) a graphics controller coupled to the CPU, is met by IMC 140 which comprises graphics engine 212 illustrated in fig.6;

c) the claimed local bus coupled to the CPU and graphics controller is met by PCI/USB Fig.2A;
d) the claimed Digital television interface that receives incoming digital TV data, is met by Decoder 172, fig. 3;
e) a local bus interface that transmits outgoing digital television data to the graphics controller over the local bus is met by I^2C bus system, fig.6;

f) the claimed memory controller that stores the incoming digital television data to one frame buffer and reading the outgoing digital television data from another frame buffer; digital television interface for receiving incoming digital television data, is met by Memory controllers 221 and 222, fig. 6;

Except for;

g) a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

h) second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

i) wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed;

Regarding g) and h), see rejection of claim 1 (a) and (b).

Regarding I), see rejection of claim 1(c).

Considering claim **9**, see rejection of claim 6.

Considering claim **10**, the claimed display device coupled to the local bus for receiving outgoing digital television data over the local bus is met by display 142, figs. 2A-2B.

Considering claim **11,** the claimed wherein the memory controller stores the incoming digital television data to the first frame buffer and reads the outgoing digital television data from the second frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the second frame buffer to the display device on a second portion of the refresh of the display device is met by memory controllers 221 and 222, fig.6;

Considering claim **12**, the claimed wherein the memory controller stores the incoming digital television data to the *second frame buffer* and reads the outgoing digital television data from the first frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the first frame buffer to the display device on a second portion of the refresh of the display device;

Regarding claim 12, see rejection of claim 1 (a) and (b).

Considering claim **13**, the claimed wherein the local bus interface monitors a refresh of display device for receiving the outgoing digital television data is met by CPU 102, fig.2;

Considering claim **14**, the claimed wherein a refresh rate of the incoming digital television data is decoupled from a refresh rate of the outgoing digital television data.

Regarding 14, see rejection of claim 1(d).

Considering claim **15**, the digital television local bus logic further comprising: a write state machine for detecting whether the incoming digital television data is being written to the first frame buffer or the second frame buffer, is met by the disclosure that "The high level graphical protocol used by the IMC 140 of the present invention eliminates many of the CPU reads and writes of graphical information that are required in prior art systems. Instead, a system incorporating an IMC 140 according to the present invention includes a high level graphical protocol whereby the CPU 102 instructs the IMC 140 to manipulate the data stored in the system memory 110...Rather, the IMC 140 reads the text data into the system memory 110, preferably in ASCII format, and

the IMC 140 processes the text data for display output. This operation is performed under the direction of the CPU 102 through the high level graphical protocol used by the IMC 140...In current prior art systems, this operation requires either extra cost for memory in the graphical subsystem, i.e., additional video memory or VRAM, or the CPU 102 is required to move the occluded information from the graphical subsystem back into the system memory for temporary storage." (col. 13, lines 29-60)

Considering claim **16**, the claimed the digital television/local bus logic further comprising: a read state machine for informing the memory controller of a frame buffer from which to read the outgoing digital television data.

Regarding claim 16, see rejection of claim 15.

Considering claim **17**, a digital television/local bus interface logic, comprising:
a) the claimed a digital television interface that receives incoming digital television data is met by the Host I/F 202, Fig.6;
b) the claimed a local bus interface that transmits outgoing digital television data to the graphics controller for display on a display device is met by PCI or USB, Fig. 2A;

e) the claimed a memory controller that stores the incoming digital television data to one frame buffer and reads the outgoing digital television data from another frame buffer on a first portion of a refresh of a display device and transmits the outgoing digital television data in the one frame buffer to the display device on a second portion of the refresh of the display device, the first and second portions of the refresh identified by a feedback signal from the graphics controller, is met by the Memory controllers 221 and 222, fig. 6; (see also rejection of claim 1(c)).

Except for;

c) the claimed a first frame buffer for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

d) the claimed a second frame buffer for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding c) and d), see rejection of claim 1 (a) and (b).

Considering claim **18**, the claimed wherein the local bus interface comprises a peripheral component interconnect (PCI) interface is met by PCI, fig.2A.

Considering claim **20,** see rejection of claim 11.

Considering claim **21,** see rejection of claim 12.

Considering claim **22,** see rejection of claim 14.

Considering claim **23,** see rejection of claim 15.

Considering claim **24,** see rejection of claim 16.

Considering claim **34**, Dye discloses the following claimed subject matter, note;

c) the claimed a means for monitoring a feedback signal provided by a means for controlling graphics, the feedback signal indicates whether a programmed position of a display device has been refreshed;

Regarding c), see rejection of claim 1(c).

d) the claimed a means for transmitting the outgoing digital television data in one of the means for storing to a means for controlling graphics for display on a display device when a programmed position of the display device is refreshed, is met by Storage FIFO 244, fig.6;

Except for;

a) the claimed storing means for storing the incoming digital television data and the outgoing digital television data in an alternating manner;

b) a second means for storing the outgoing digital television data and the incoming digital television data in an alternating manner;

Regarding a) and b), see rejection of claim 1(a) and (b).

Considering claim **35**, a means for reading the outgoing digital television data from a storing means is met by display storage FIFO 244, fig.6; (see also rejection of claim 1 (a) and (b))

Considering claim **36**, the claimed means for monitoring a horizontal sync and a vertical sync of the display device is met by the disclosure "The IMC 140 preferably generates red, green, blue (RGB) signals as well as vertical and horizontal synchronization signals for generating images on the display 142." (col. 10, lines 49-52)

Considering claim **37**, the claimed a means for detecting whether the outgoing digital television data is stored in the first means for storing or the second for storing, is met by CPU 102, FIG.3; (see col. 13, lines 29-60 and rejection of claim 34(a) and (b))

Considering claim **38**, see rejection of claim 6.

Considering claim **40**, Dye discloses the following claimed subject matter, note;

a) a central processing unit (CPU), is met by CPU 102 (FIG.2A).

b) the claimed local bus coupled to the CPU, is met by PCI/USB, Fig. 2A/2B, which, given reasonably broad interpretation, is coupled to the CPU through 140.

c) the claimed graphics controller coupled to the local bus, is met by IMC 140, Fig. 2A+ which comprises a graphics engine 210 as illustrated in fig.6.

d) the claimed display device for receiving outgoing digital television data from the graphics controller is met by display 142, Fig. 2A;

e) the claimed digital television/local bus interface logic coupled to the local bus for storing incoming digital television data and the outgoing digital television data and selectively providing the outgoing digital television data over the local bus to the graphics controller when a programmed position of the display device is refreshed, is met by Interactive Media Controller 140 and System Memory 110, Fig. 2A;

As for the newly added limitation, wherein the graphics controller provides a feedback signal to the digital television/local bus interface logic to indicate whether a display device is refreshed, see rejection of claim 1 (c).

Considering claim **41**, the claimed core logic coupled between the local bus and the graphics controller is met by Bus I/F logic 202, figs. 5 and 6;

Considering claim **42**, the claimed digital television decoder for providing incoming television data to the digital television/local bus interface logic is met by decoder 172, Fig.3;

Considering claim **43**, the claimed digital television tuner for providing incoming digital television data to the digital television decoder, is inherent in televisions system such as Dye's (see the television system Fig.1B);

Considering claim **44**, see rejection of claim 1;

Considering claim **45**, wherein the feedback signal comprises a horizontal sync and a vertical sync of the display device, is implied because without the vertical and horizontal sync signals the position of the data signals may not be controlled properly.

Considering claim **46**, the claimed wherein the local bus comprises a peripheral component interconnect (PCI) bus, is met by PCI (fig.2A).

Response to Arguments

Applicant's Argument

Dye does not teach or fairly suggest a feedback signal from a graphics controller and that feedback signal indicates whether a programmed position of the display device has been refreshed. (claims 1, 8, 34, and 40) Dye does not teach or fairly suggest a feedback signal from a graphics controller, or a feedback signal that identifies the first and second portions of the refresh (claims 17).

Examiner's Response

The Abstract of the disclosure states: A graphics controller (IMC) which performs pointer-based and/or display list-based video refresh operations that enable screen refresh data to be assembled on a per window or per object basis, thereby greatly increasing the performance of the graphical display. It is also well known in the art that controllers (such as the claimed graphics controller) utilize the sync signal (Vsync/Hsync) to control the position of the video signal or other data displayed on the display screen, or to synchronize the video data with the audio data, etc. In this case, the Integrated Memory controller 140 as illustrated on Figs. 5 and 6, combines the I/F logic, memory control, graphics engine and storage capacities, allowing the IMC to perform refresh operations. See rejection of claims above.

Allowable Subject Matter

4. Claims **48-52** are allowable over the cited prior art.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a dual stream digital television/local bus interface logic, comprising: a first digital television interface for receiving a first incoming digital television data stream; a second digital television interfaceœ for receiving a second incoming digital television data stream, a local bus interlace for transmitting a first outgoing digital data stream and a second outgoing digital television data stream, a first frame buffer for storing the first incoming digital television data stream and the first outgoing digital television data stream in an alternating manner, a second frame buffer for storing the first outgoing digital television data stream and the first incoming digital television data stream in an alternating manner a third frame buffer for storing the second incoming digital television data stream and the second outgoing digital television data stream in an alternating manner a fourth frame buffer for storing the second outgoing digital television data stream and the second Incoming digital television data stream in an alternating manner; and a memory controller for storing the first incoming digital television data stream to the first frame buffer or the second frame buffer and reading the first outgoing digital television data stream from the second frame buffer or the first frame buffer on a first portion of a refresh of a display device, storing the second incoming digital television data stream to the third frame buffer or the fourth frame buffer and reading the second outgoing digital television data stream from the fourth frame buffer or the third frame buffer on the first portion of Me refresh of the display device, transmitting the first outgoing digital' television data stream to the display device on a second portion of the refresh of the display device, and transmitting the second

outgoing digital television data stream to the display device on the second portion of the refresh of the display device. as in claim **48**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
February 15, 2005

PAULOS M. NATNAEL
PATENT EXAMINER